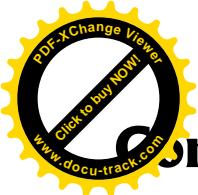


萬力電子有限公司
WANLI ELECTRONIC CO. LTD.

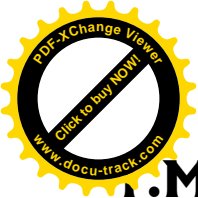
WW320240A-TMI-VZ#

樣品承認書

APPROVED BY: _____



1. Module classification information
2. Precautions in Use of LCM
3. General Specification
4. Absolute Maximum Ratings
5. Electrical Characteristics
6. Optical Characteristics
7. Interface Pin Function
8. Contour Drawing & Block Diagram
9. Timing Characteristics
10. Reliability
11. Backlight Information
12. Inspection specification
13. Material List of Components for RoHs



1. Module Classification Information

W G 3 2 0 2 4 0 A — T M I — VZ#
 ① ② ③ ④ ⑤ ⑥ ⑦ ⑧

① Brand : WINSTAR DISPLAY CORPORATION

② Display Type : H→Character Type, G→Graphic Type

③ Display Font : 320 * 240 Dots

④ Model serials number

⑤ Backlight Type :

N→Without backlight	T→LED, White
B→EL, Blue green	A→LED, Amber
D→EL, Green	R→LED, Red
W→EL, White	O→LED, Orange
F→CCFL, White	G→LED, Green
Y→LED, Yellow Green	B→LED, Blue

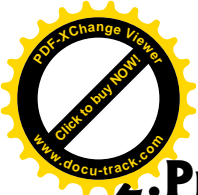
⑥ LCD Mode :

B→TN Positive, Gray	T→FSTN Negative
N→TN Negative,	
G→STN Positive, Gray	
Y→STN Positive, Yellow Green	
M→STN Negative, Blue	
F→FSTN Positive	

⑦ LCD Polarize Type/
 Temperature range/
 View direction

A→Reflective, N.T, 6:00	H→Transflective, W.T,6:00
D→Reflective, N.T, 12:00	K→Transflective,W.T,12:00
G→Reflective, W. T, 6:00	C→Transmissive, N.T,6:00
J→Reflective, W. T, 12:00	F→Transmissive, N.T,12:00
B→Transflective, N.T,6:00	I→Transmissive, W. T, 6:00
E→Transflective, N.T.12:00	L→Transmissive, W.T,12:00

⑧ Special Code V: Bulid in Negative Voltage; Z:ICNT7086
 #:Fit in with the ROHS Directions and regulations

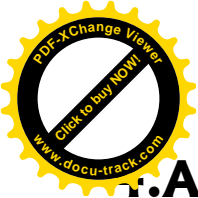


2. Precautions in Use of LCD Module

- (1) Avoid applying excessive shocks to the module or making any alterations or modifications to it.
- (2) Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD Module.
- (3) Don't disassemble the LCM.
- (4) Don't operate it above the absolute maximum rating.
- (5) Don't drop, bend or twist LCM.
- (6) Soldering: only to the I/O terminals.
- (7) Storage: please storage in anti-static electricity container and clean environment.
- (8) Winstar have the right to change the passive components
- (9) Winstar have the right to change the PCB Rev.

3. General Specification

ITEM	STANDARD VALUE	UNIT
Number of dots	320x240	dots
Outline dimension	160.0(W)x 109.0(H)x 13.0max(T)	mm
View area	122.0(W)x 92.0(H)	mm
Active area	115.18(W)x 86.38(H)	mm
Dot size	0.34(W)x 0.34(H)	mm
Dot pitch	0.36(W)x 0.36(H)	mm
LCD type	STN Negative, Transmissive ,Blue (In LCD production, It will occur slightly color difference. We can only guarantee the same color in the same batch.)	
View direction	6 o'clock	
Backlight	LED , White	



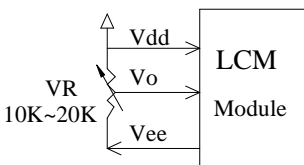
4. Absolute Maximum Ratings

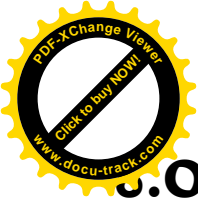
ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating Temperature	T_{OP}	-20	—	+70	°C
Storage Temperature	T_{ST}	-30	—	+80	°C
Input Voltage	V_I	0	—	V_{DD}	V
Supply Voltage For Logic	V_{DD}	0	—	6.5	V
Supply Voltage For LCD	$V_{DD}-V_{EE}$	0	—	32	V

5. Electrical Characteristics

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Logic Voltage	$V_{DD}-V_{SS}$	—	2.7	—	5.5	V
Supply Voltage For LCD	$V_{DD}-V_O$	$T_a=-20^{\circ}C$	—	—	26.2	V
		$T_a=25^{\circ}C$	—	24.0	—	V
*Note		$T_a=+70^{\circ}C$	22.1	—	—	V
Input High Volt.	V_{IH}	—	0.8VDD	—	VDD	V
Input Low Volt.	V_{IL}	—	-0.3	—	0.2VDD	V
Output High Volt.	V_{OH}	—	VDD -0.4	—	VDD	V
Output Low Volt.	V_{OL}	—	0	—	0.4	V
Supply Current	I_{DD}	—	70.0	75.0	80.0	mA

*Note: Please design the VOP adjustment circuit on customer's main board



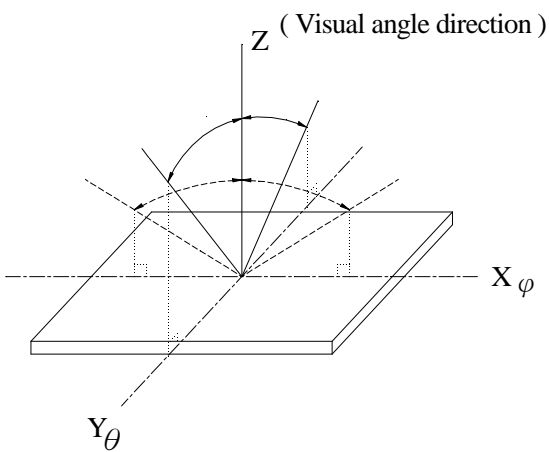


Optical Characteristics

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
View Angle	(V) θ	$CR \geq 2$	20	—	40	deg.
	(H) φ	$CR \geq 2$	-30	—	30	deg.
Contrast Ratio	CR	—	—	3	—	—
Response Time	T rise	—	—	200	300	ms
	T fall	—	—	150	200	ms

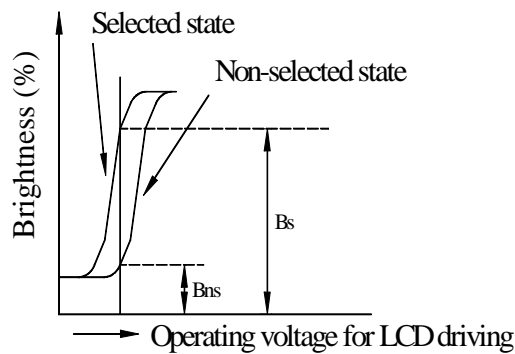
6.1 Definitions

View Angles



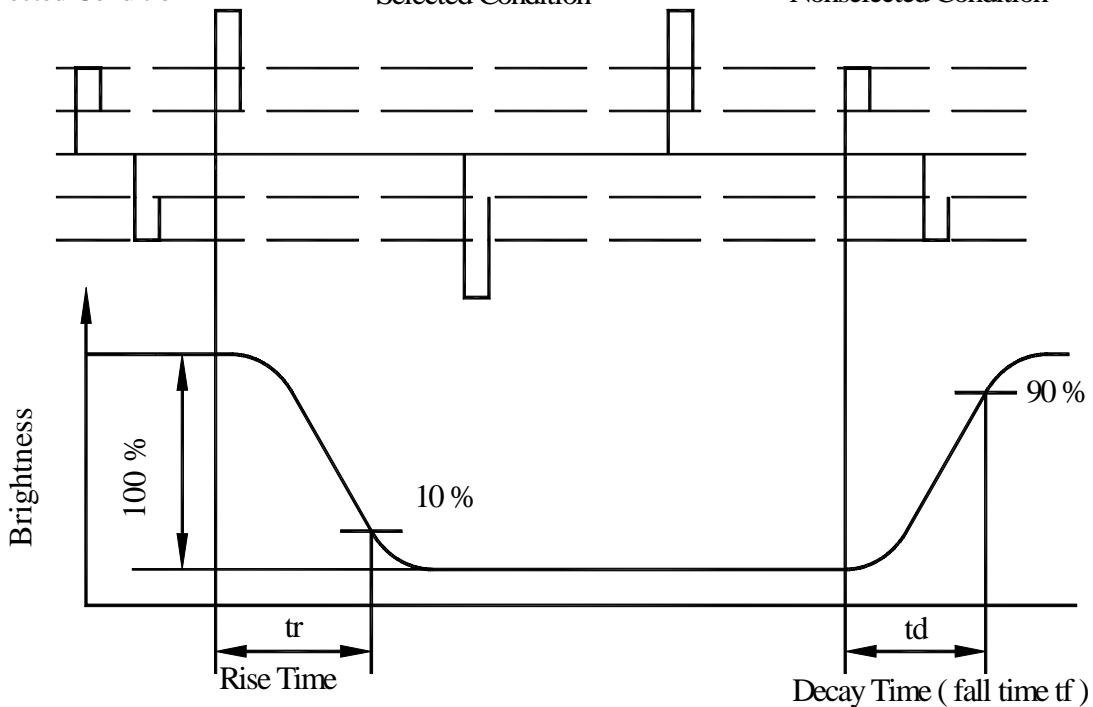
Contrast Ratio

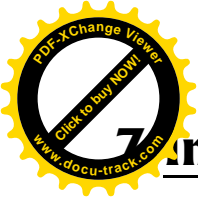
$$CR = \frac{\text{Brightness at selected state (BS)}}{\text{Brightness at non-selected state (Bns)}}$$



Response time

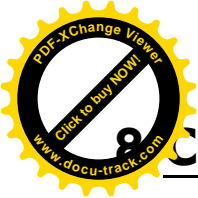
Nonselected Condition Selected Condition Nonselected Condition



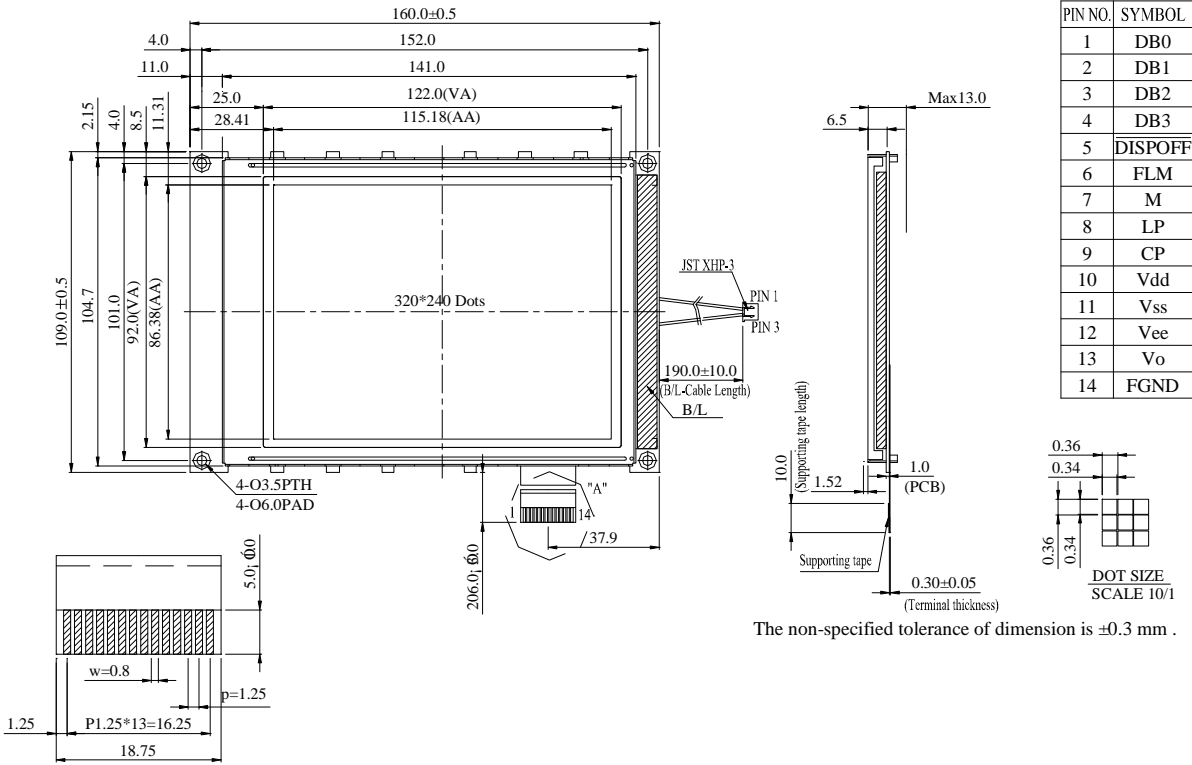


Interface Description

Pin No.	Symbol	Level	Description
1	D0	H/L	Data bus line
2	D1	H/L	Data bus line
3	D2	H/L	Data bus line
4	D3	H/L	Data bus line
5	<u>DISPOFF</u>	H/L	H: Display ON, L: Display OFF
6	FLM	H/L	Scan start-up signal
7	M(N.C.)	H/L	Frame reverse signal(alternate signal)
8	CL1(LP)	H to L	Data latch pulse
9	CL2(CP)	H to L	Data shift pulse
10	V _{DD}	5.0V	Power supply for Logic
11	V _{SS}	0V	Ground
12	V _{EE}	V	Negative voltage output (Built-in)
13	V _O	(Variable)	Driving voltage for LCD
14	FGND		Frame Ground

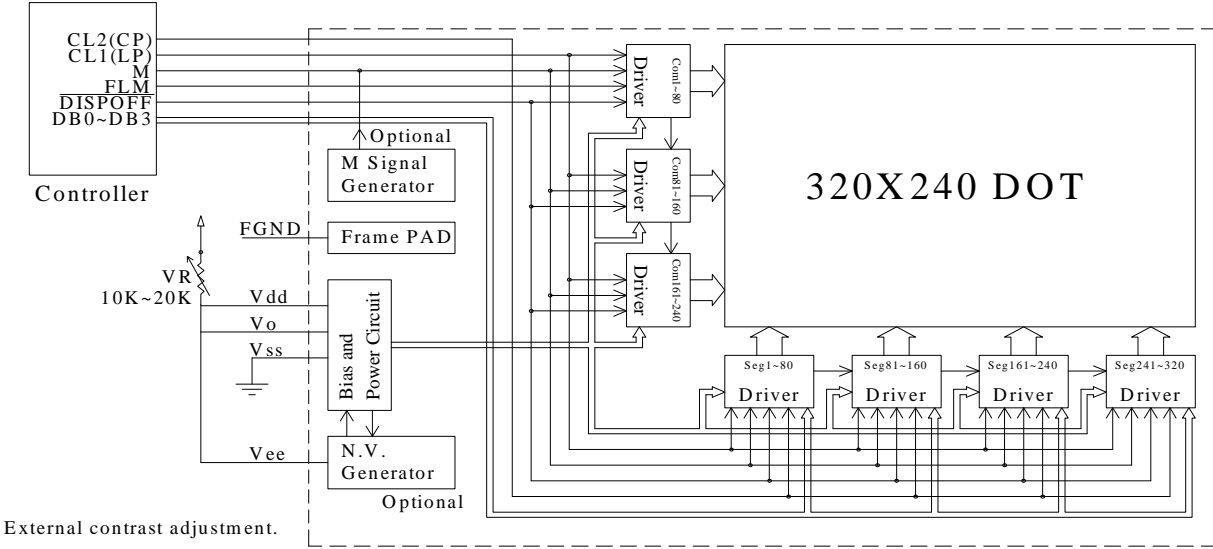


Contour Drawing & Block diagram

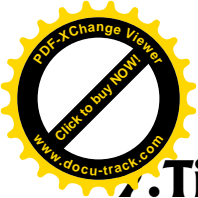


The non-specified tolerance of dimension is ±0.3 mm .

The stiffen tape of the FFC cable is in the same direction as LCD panel side, and its contact side as PCB component's side



COM	D3	D2	D1	D0	D3	D2	D1	D0
COM001	D3	D2	D1	D0	D3	D2	D1	D0
COM002	D3	D2	D1	D0	D3	D2	D1	D0
.....
COM 239	D3	D2	D1	D0	D3	D2	D1	D0
COM 240	D3	D2	D1	D0	D3	D2	D1	D0
SEG001
SEG002
SEG003
SEG004
.....
SEG317
SEG318
SEG319
SEG320



Timing Characteristics

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

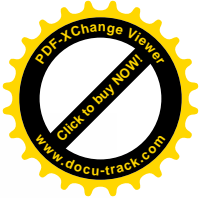
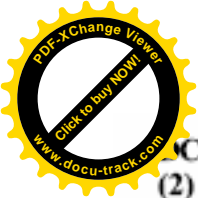
(1) Segment Driver Application

(V_{SS} = 0V, T_a = -30 ~ +85°C)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit	
Operating Voltage 1	V _{DD}	-	2.7	-	5.5	V	
	V _{LCD}	V _N = V _{DD} - V _{EE}	6	-	28		
Input voltage (1)	V _{IH}	-	0.8V _{DD}	-	V _{DD}		
	V _{IL}	-	0	-	0.2V _{DD}		
Input voltage (2)	V _{OH}	I _{CH} = -0.4mA	V _{DD} - 0.4	-	-	V	
	V _{OL}	I _{OH} = -0.4mA	-	-	0.4		
Input leakage current 1 (1)	I _{IL1}	V _{IN} = V _{DD} to V _{SS}	-10	-	10	μA	
Input leakage current 2 (3)	I _{IL2}	V _N = V _{DD} to V _{EE}	-25	-	25		
On resistance(4)	R _{ON}	I _{ON} = 100 μA	-	2	4	kΩ	
Supply current(5)	I _{STBY}	f _{CL1} = 32kHz, M = V _{SS}	V _{SS} PIN	-	-	100	μA
	I _{DD}	f _{CL1} = 32kHz F _M = 80HZ	V _{DD} = 5V	-	-	5	mA
			V _{DD} = 3V	-	-	2	
I _{EE}		V _{DD} = 5V	-	-	500	μA	

NOTES:

- Applied to CL1, CL2, ELB, ERB, D1_SID - D4_DR, SHL, DISPOFFB, M, CS, AMS pin
 - ELB, ERB pin
 - V0, V12, V43, V5 pin
 - V_{LCD} = V_{DD} - V_{EE} V0 = V_{DD} = 5V, V5 = V_{EE} = -23 V
V12 = V_{DD} - 2/n(V_{LCD}), V43 = V_{EE} + 2/n(V_{LCD}), n = 17 (1/256 duty, 1/17 bias)
 - V0 = V_{DD}, V12 = 1.71V (V_{DD} = 5V) or -0.06V (V_{DD} = 3V),
V43 = -19.71 V (V_{DD} = 5V) or -19.94V (V_{DD} = 3V), V5 = V_{EE} = -23V, no-load condition (1/256 duty, 1/17 bias)
- 4-bit parallel interface mode
I_{STBY}: V_{DD} = 5V, f_{CL2} = 5.12MHz, SHL = V_{SS}, DISPOFFB = V_{DD}, M = V_{SS}, display data pattern = 0000
I_{DD}: V_{DD} = 3V, f_{CL2} = 4MHz, display data pattern = 0101
V_{DD} = 5 V, f_{CL2} = 5.12MHz, display data pattern = 0101
I_{EE}: V_{DD} = 5V, f_{CL2} = 5.12MHz, display data pattern = 0101, V_{EE} pin



DC CHARACTERISTICS (CONTINUED)

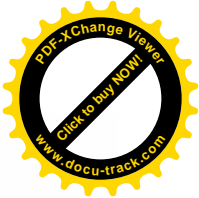
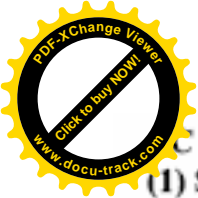
(2) Common Driver Application

($V_{SS} = 0V, T_a = -30 \sim +85^\circ C$)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit	
Operating Voltage 1	V_{DD}	-	2.7	-	5.5	V	
	V_{LCD}	$V_{IN} = V_{DD} - V_{EE}$	6	-	28		
Input voltage (1)	V_{IH}	-	$0.8V_{DD}$	-	V_{DD}		
	V_{IL}	-	0	-	$0.2V_{DD}$		
Input voltage (3)	V_{OH}	$I_{CH} = -0.4mA$	$V_{DD} - 0.4$	-	-	V	
	V_{OL}	$I_{OH} = -0.4mA$	-	-	0.4		
Input leakage current 1 (1)	I_{IL1}	$V_{IN} = V_{DD}$ to V_{SS}	-10	-	10	μA	
Input leakage current 2 (2)	I_{IL2}	$V_{IN} = 0V, V_{DD} = 5V$ (Pull up)	-50	-125	-250		
Input leakage current 3 (4)	I_{IL3}	$V_{IN} = V_{DD}$ to V_{EE}	-25	-	25		
On resistance(5)	R_{ON}	$I_{ON} = 100 \mu A$	-	2	4	$k\Omega$	
Supply current(6)	I_{STBY}	$f_{CL1} = 32kHz, M = V_{SS}$	V_{SS} PIN	-	-	100	μA
	I_{DD}	$f_{CL1} = 32kHz, F_M = 80Hz$	$V_{DD} = 5V$	-	-	200	
			$V_{DD} = 3V$	-	-	120	
			$V_{DD} = 5V$	-	-	150	

NOTES:

- Applied to CL1, D2_DL (SHL = LOW), D4_DR (SHL = HIGH), SHL, DISPOFFB, M, CS, AMS pin
 - Pull-up input pins : CL2, D1_SID, D3_DM (AMS = HIGH), ELB (SHL = LOW), ERB (SHL = HIGH)
 - D2_DL (SHL = HIGH), D4_DR (SHL = LOW) pin
 - V0, V12, V43, V5 pin
 - $V_{LCD} = V_{DD} - V_{EE}$, $V0 = V_{DD} = 5V$, $V5 = V_{EE} = -23V$
 $V12 = V_{DD} - 1/n(V_{LCD})$, $V43 = V_{EE} + 1/n(V_{LCD})$, $n = 17$ (1/256 duty, 1/17 bias)
 - $V0 = V_{DD}$, $V12 = 3.35V$ ($V_{DD} = 5V$) or $1.47V$ ($V_{DD} = 3V$),
 $V43 = -21.35V$ ($V_{DD} = 5V$) or $-21.47V$ ($V_{DD} = 3V$), $V5 = V_{EE} = -23V$, no-load condition (1/256 duty, 1/17 bias)
- single-type mode operation : AMS = V_{SS} , SHL = V_{EE} , DISPOFFB = V_{DD}
D1_SID = D3_DM = VDD, D4_DR = OPEN, ELB = ERB = OPEN,
 I_{STBY} : $V_{DD} = 5V, M = V_{SS}, D2_DL = V_{SS}$
 I_{DD} : $f_M = 80Hz, D2_DL = V_{DD}$
 $V_{DD} = 3V$, display data pattern = 10000000..., 01000000..., 00100000..., 00010000..., ..
 $V_{DD} = 5V$, display data pattern = 10000000..., 01000000..., 00100000..., 00010000..., ..
 I_{EE} : $f_M = 80Hz, D2_DL = V_{DD}$
 $V_{DD} = 5V$, current through V_{EE} Pin, display data pattern = 10000000..., 01000000..., 00100000..., 00010000...



CHARACTERISTICS

(1) Segment Driver Application

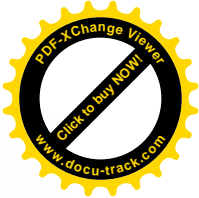
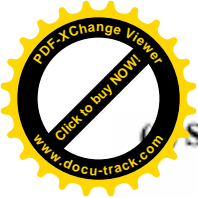
($V_{SS} = 0V$, $T_a = -30 \sim +85^\circ C$)

Characteristic	Symbol	Test condition	(1) VDD=5V±10%			(2) VDD=3V±10%			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock cycle time	t_{CY}	Duty=50%	125	-	-	250	-	-	ns
Clock pulse width	t_{WCK}	-	45	-	-	95	-	-	
Clock rise/ fall time	t_R / t_F	-	-	-	-	-	-	30	
Data set-up time	t_{DS}	-	30	-	-	65	-	-	
Data hold time	t_{DH}	-	30	-	-	65	-	-	
Clock set-up time	t_{CS}	-	80	-	-	120	-	-	
Clock hold time	t_{CH}	-	80	-	-	120	-	-	
Propagation delay time	t_{PHL}	ELB output	-	-	60	-	-	125	
		ERB output	-	-	60	-	-	125	
ELB,ERB set-up time	t_{FSU}	ELB input	30	-	-	65	-	-	
		ERB input	30	-	-	65	-	-	
DISPOFFB low pulse width	t_{WDL}	-	1.2	-	-	1.2	-	-	μs
DISPOFFB clear time	t_{CD}	-	100	-	-	100	-	-	ns
M – OUT propagation delay time	t_{PD1}	$C_L=15pF$	-	-	1.0	-	-	1.2	μs
CL1 – OUT propagation delay time	t_{PD2}		-	-	1.0	-	-	1.2	
DISPOFFB – OUT propagation delay time	t_{PD3}		-	-	1.0	-	-	-	

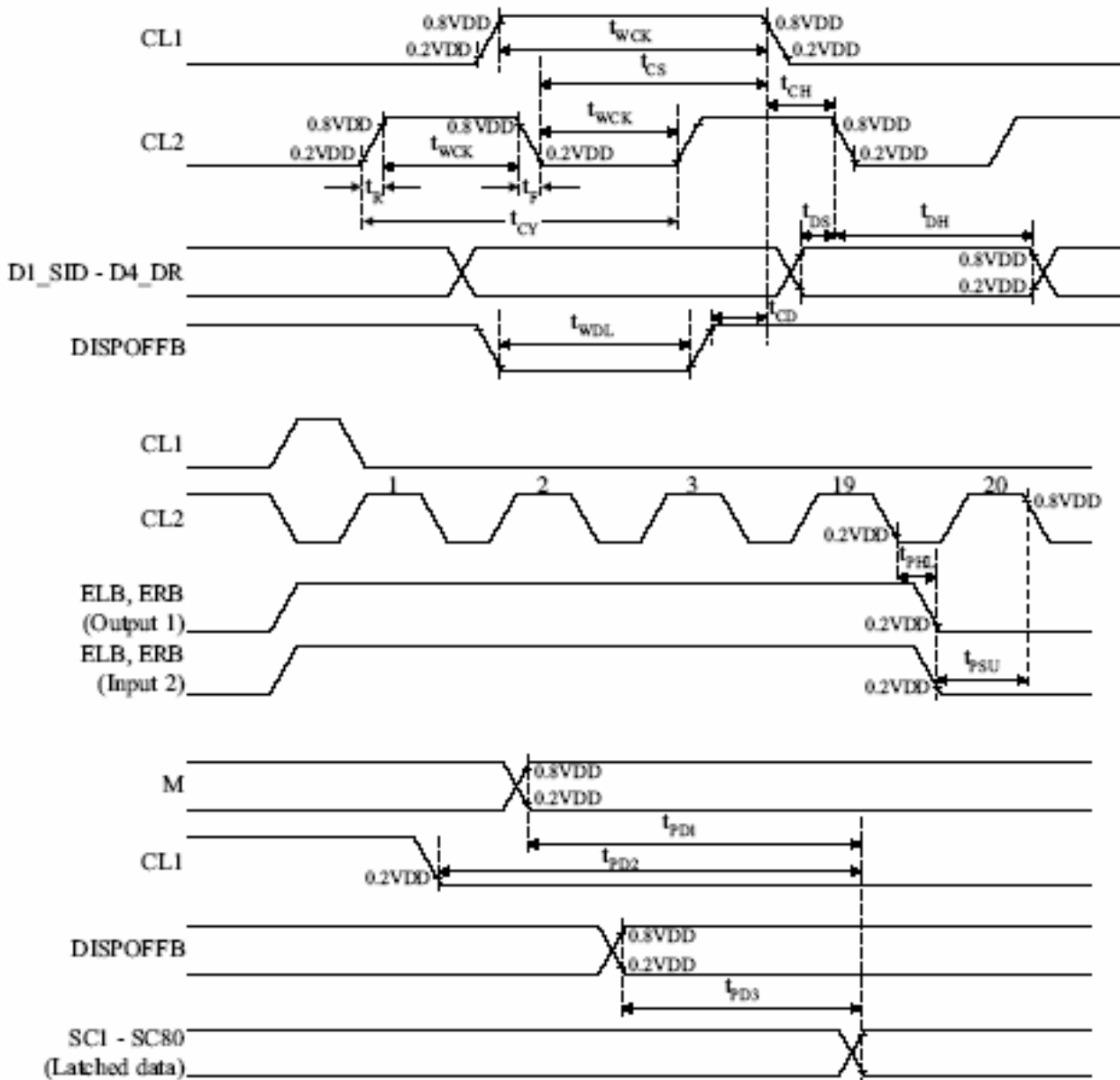
(2) Common Driver Application

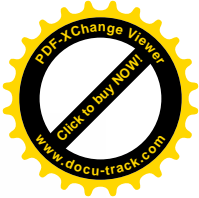
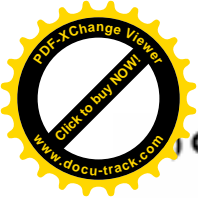
($V_{SS} = 0V$, $T_a = -30 \sim +85^\circ C$)

Characteristic	Symbol	Test condition	(1) VDD=5V±10%			(2) VDD=3V±10%			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock cycle time	t_{CY}	Duty=50%	250	-	-	500	-	-	ns
Clock pulse width	t_{WCK}	-	45	-	-	95	-	-	
Clock rise/ fall time	t_R / t_F	-	-	-	50	-	-	50	
Data set-up time	t_{DS}	-	30	-	-	65	-	-	
Data hold time	t_{DH}	-	30	-	-	65	-	-	
DISPOFFB low pulse width	t_{WDL}	-	1.2	-	-	1.2	-	-	μs
DISPOFFB clear time	t_{CD}	-	100	-	-	100	-	-	ns
Output delay time	t_{DL}	$C_L=15pF$	-	-	200	-	-	250	μs
M – OUT propagation delay time	t_{PD1}		-	-	1.0	-	-	1.2	
CL1 – OUT propagation delay time	t_{PD2}		-	-	1.0	-	-	1.2	
DISPOFFB – OUT propagation delay time	t_{PD3}		-	-	1.0	-	-	1.2	

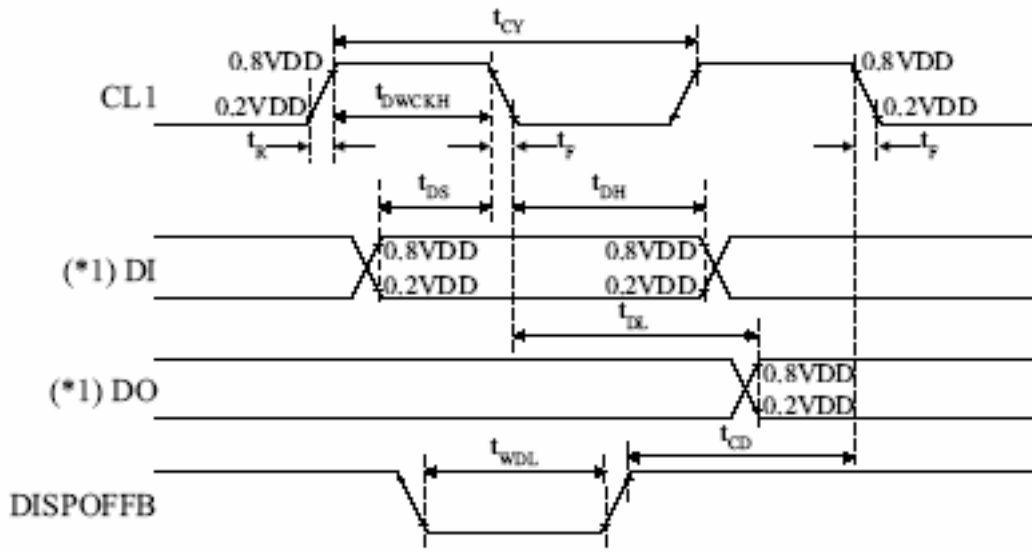


Segment Driver Application Timing

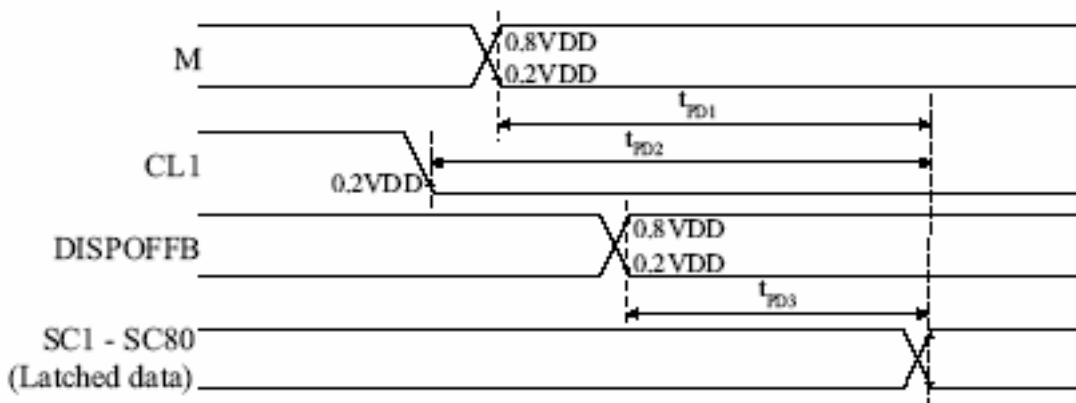


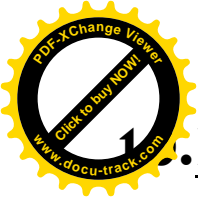


Common Driver Application Timing



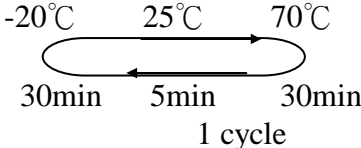
(*1) When in single-type interface mode
 DI=>DDL(SHL=L), D4_DR(SHL=H)
 DO=>D4_DR(SHL=L), D2_DL(SHL=H)
 When in dual-type interface mode
 DI=>D2_DL and D3_DM(SHL=L), D4_DR and D3_DM(SHL=H)
 DO=>D4_DR(SHL=L), D2_DL(SHL=H)





RELIABILITY

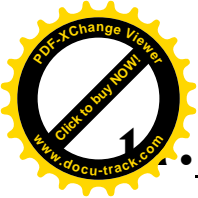
Content of Reliability Test (wide temperature, -20°C~70°C)

Environmental Test			
Test Item	Content of Test	Test Condition	Note
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80°C 200hrs	2
Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-30°C 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70°C 200hrs	—
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20°C 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60 °C,90%RH max For 96hrs under no-load condition excluding the polarizer, Then taking it out and drying it at normal temperature.	60°C,90%RH 96hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of operation  1 cycle	-20°C/70°C 10 cycles	—
Vibration test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	3
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V,RS=1.5kΩ CS=100pF 1 time	—

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.

Note3: Vibration test will be conducted to the product itself without putting it in a container.



Backlight Information

Specification

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITION
Supply Current	I _{LED}	115.2	128	200	mA	V=3.5V
Supply Voltage	V	3.4	3.5	3.6	V	—
Reverse Voltage	V _R	—	—	5	V	—
Luminous Intensity	I _V	260	280	—	CD/M ²	I _{LED} =128mA
Wave Length	λ _p	—	—	—	nm	I _{LED} =128mA
LED Life Time (For Reference only)	—	—	50K	—	Hr.	I _{LED} ≤ 128 25°C, 50-60%RH, (Note 1)
Color	White					

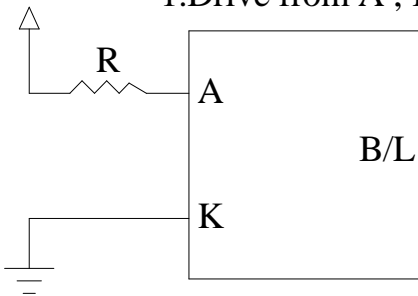
* The LED of B/L is drive by current only, drive voltage is for reference only.

drive voltage can make driving current under safety area (current between minimum and maximum).

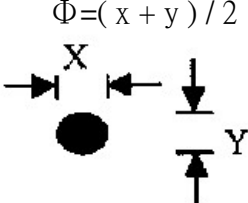
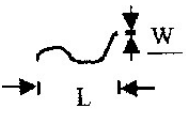
Note1 :50K hours is only an estimate for reference.

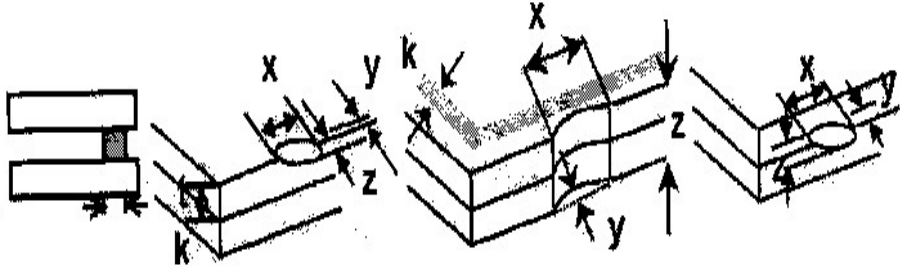
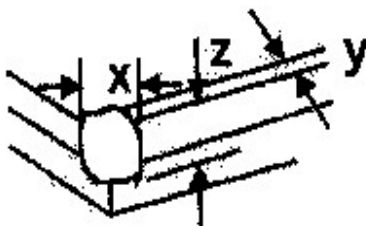
LED B\L Drive Method

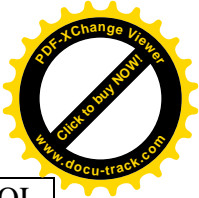
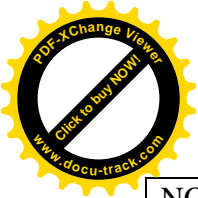
1. Drive from A , K

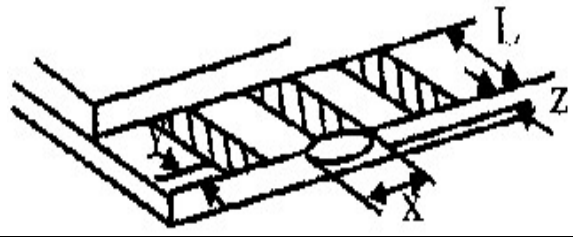
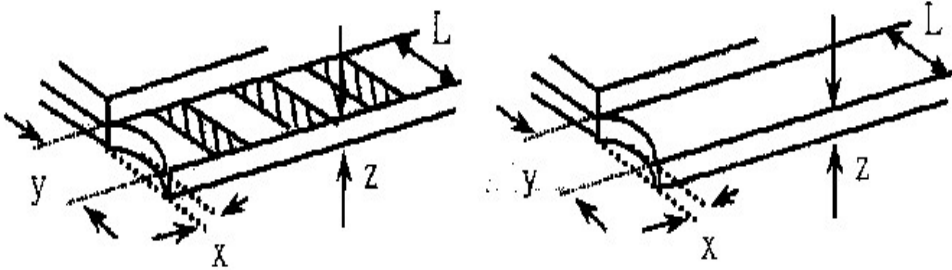
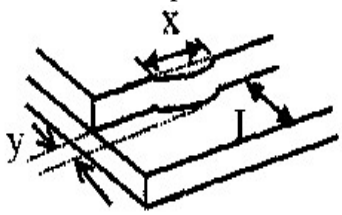


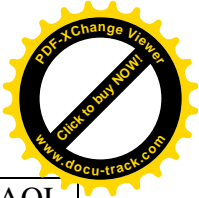
2. Inspection specification

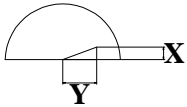
NO	Item	Criterion	AQL												
01	Electrical Testing	1.1 Missing vertical, horizontal segment, segment contrast defect. 1.2 Missing character, dot or icon. 1.3 Display malfunction. 1.4 No function or no display. 1.5 Current consumption exceeds product specifications. 1.6 LCD viewing angle defect. 1.7 Mixed product types. 1.8 Contrast defect.	0.65												
02	Black or white spots on LCD (display only)	2.1 White and black spots on display $\leq 0.25\text{mm}$, no more than three white or black spots present. 2.2 Densely spaced: No more than two spots or lines within 3mm	2.5												
03	LCD black spots, white spots, contamination (non-display)	3.1 Round type : As following drawing $\Phi = (x + y) / 2$  <table border="1" data-bbox="858 945 1337 1160"> <thead> <tr> <th>SIZE</th> <th>Acceptable Q TY</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.10$</td> <td>Accept no dense</td> </tr> <tr> <td>$0.10 < \Phi \leq 0.20$</td> <td>2</td> </tr> <tr> <td>$0.20 < \Phi \leq 0.25$</td> <td>1</td> </tr> <tr> <td>$0.25 < \Phi$</td> <td>0</td> </tr> </tbody> </table>	SIZE	Acceptable Q TY	$\Phi \leq 0.10$	Accept no dense	$0.10 < \Phi \leq 0.20$	2	$0.20 < \Phi \leq 0.25$	1	$0.25 < \Phi$	0	2.5		
		SIZE	Acceptable Q TY												
$\Phi \leq 0.10$	Accept no dense														
$0.10 < \Phi \leq 0.20$	2														
$0.20 < \Phi \leq 0.25$	1														
$0.25 < \Phi$	0														
3.2 Line type : (As following drawing)  <table border="1" data-bbox="694 1236 1337 1451"> <thead> <tr> <th>Length</th> <th>Width</th> <th>Acceptable Q TY</th> </tr> </thead> <tbody> <tr> <td>---</td> <td>$W \leq 0.02$</td> <td>Accept no dense</td> </tr> <tr> <td>$L \leq 3.0$</td> <td>$0.02 < W \leq 0.03$</td> <td rowspan="2">2</td> </tr> <tr> <td>$L \leq 2.5$</td> <td>$0.03 < W \leq 0.05$</td> </tr> <tr> <td>---</td> <td>$0.05 < W$</td> <td>As round type</td> </tr> </tbody> </table>	Length	Width	Acceptable Q TY	---	$W \leq 0.02$	Accept no dense	$L \leq 3.0$	$0.02 < W \leq 0.03$	2	$L \leq 2.5$	$0.03 < W \leq 0.05$	---	$0.05 < W$	As round type	2.5
Length	Width	Acceptable Q TY													
---	$W \leq 0.02$	Accept no dense													
$L \leq 3.0$	$0.02 < W \leq 0.03$	2													
$L \leq 2.5$	$0.03 < W \leq 0.05$														
---	$0.05 < W$	As round type													
04	Polarizer bubbles	If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction. <table border="1" data-bbox="826 1500 1337 1758"> <thead> <tr> <th>Size Φ</th> <th>Acceptable Q TY</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.20$</td> <td>Accept no dense</td> </tr> <tr> <td>$0.20 < \Phi \leq 0.50$</td> <td>3</td> </tr> <tr> <td>$0.50 < \Phi \leq 1.00$</td> <td>2</td> </tr> <tr> <td>$1.00 < \Phi$</td> <td>0</td> </tr> <tr> <td>Total Q TY</td> <td>3</td> </tr> </tbody> </table>	Size Φ	Acceptable Q TY	$\Phi \leq 0.20$	Accept no dense	$0.20 < \Phi \leq 0.50$	3	$0.50 < \Phi \leq 1.00$	2	$1.00 < \Phi$	0	Total Q TY	3	2.5
Size Φ	Acceptable Q TY														
$\Phi \leq 0.20$	Accept no dense														
$0.20 < \Phi \leq 0.50$	3														
$0.50 < \Phi \leq 1.00$	2														
$1.00 < \Phi$	0														
Total Q TY	3														

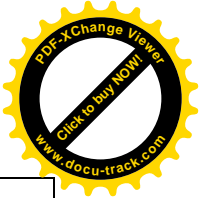
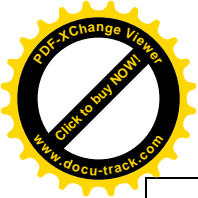
NO	Item	Criterion	AQL																		
05	Scratches	Follow NO.3 LCD black spots, white spots, contamination																			
06	Chipped glass	<p>Symbols Define: x: Chip length y: Chip width z: Chip thickness k: Seal width t: Glass thickness a: LCD side length L: Electrode pad length:</p> <p>6.1 General glass chip : 6.1.1 Chip on panel surface and crack between panels:</p>  <table border="1" data-bbox="427 1093 1337 1288"> <tr> <td>z: Chip thickness</td> <td>y: Chip width</td> <td>x: Chip length</td> </tr> <tr> <td>$Z \leq 1/2t$</td> <td>Not over viewing area</td> <td>$x \leq 1/8a$</td> </tr> <tr> <td>$1/2t < z \leq 2t$</td> <td>Not exceed 1/3k</td> <td>$x \leq 1/8a$</td> </tr> </table> <p>⊙If there are 2 or more chips, x is total length of each chip.</p> <p>6.1.2 Corner crack:</p>  <table border="1" data-bbox="427 1769 1337 1964"> <tr> <td>z: Chip thickness</td> <td>y: Chip width</td> <td>x: Chip length</td> </tr> <tr> <td>$Z \leq 1/2t$</td> <td>Not over viewing area</td> <td>$x \leq 1/8a$</td> </tr> <tr> <td>$1/2t < z \leq 2t$</td> <td>Not exceed 1/3k</td> <td>$x \leq 1/8a$</td> </tr> </table> <p>⊙If there are 2 or more chips, x is the total length of each chip.</p>	z: Chip thickness	y: Chip width	x: Chip length	$Z \leq 1/2t$	Not over viewing area	$x \leq 1/8a$	$1/2t < z \leq 2t$	Not exceed 1/3k	$x \leq 1/8a$	z: Chip thickness	y: Chip width	x: Chip length	$Z \leq 1/2t$	Not over viewing area	$x \leq 1/8a$	$1/2t < z \leq 2t$	Not exceed 1/3k	$x \leq 1/8a$	2.5
z: Chip thickness	y: Chip width	x: Chip length																			
$Z \leq 1/2t$	Not over viewing area	$x \leq 1/8a$																			
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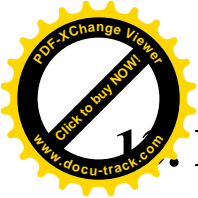
NO	Item	Criterion	AQL																
06	Glass crack	<p>Symbols :</p> <p>x: Chip length y: Chip width z: Chip thickness k: Seal width t: Glass thickness a: LCD side length L: Electrode pad length</p> <p>6.2 Protrusion over terminal :</p> <p>6.2.1 Chip on electrode pad :</p>  <table border="1" data-bbox="335 728 1252 817"> <tr> <td>y: Chip width</td> <td>x: Chip length</td> <td>z: Chip thickness</td> </tr> <tr> <td>$y \leq 0.5\text{mm}$</td> <td>$x \leq 1/8a$</td> <td>$0 < z \leq t$</td> </tr> </table> <p>6.2.2 Non-conductive portion:</p>  <table border="1" data-bbox="406 1142 1252 1232"> <tr> <td>y: Chip width</td> <td>x: Chip length</td> <td>z: Chip thickness</td> </tr> <tr> <td>$y \leq L$</td> <td>$x \leq 1/8a$</td> <td>$0 < z \leq t$</td> </tr> </table> <p>⊙If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.</p> <p>⊙If the product will be heat sealed by the customer, the alignment mark not be damaged.</p> <p>6.2.3 Substrate protuberance and internal crack.</p>  <table border="1" data-bbox="742 1489 1252 1579"> <tr> <td>y: width</td> <td>x: length</td> </tr> <tr> <td>$y \leq 1/3L$</td> <td>$x \leq a$</td> </tr> </table>	y: Chip width	x: Chip length	z: Chip thickness	$y \leq 0.5\text{mm}$	$x \leq 1/8a$	$0 < z \leq t$	y: Chip width	x: Chip length	z: Chip thickness	$y \leq L$	$x \leq 1/8a$	$0 < z \leq t$	y: width	x: length	$y \leq 1/3L$	$x \leq a$	2.5
y: Chip width	x: Chip length	z: Chip thickness																	
$y \leq 0.5\text{mm}$	$x \leq 1/8a$	$0 < z \leq t$																	
y: Chip width	x: Chip length	z: Chip thickness																	
$y \leq L$	$x \leq 1/8a$	$0 < z \leq t$																	
y: width	x: length																		
$y \leq 1/3L$	$x \leq a$																		



NO	Item	Criterion	AQL
07	Cracked glass	The LCD with extensive crack is not acceptable.	2.5
08	Backlight elements	8.1 Illumination source flickers when lit. 8.2 Spots or scratched that appear when lit must be judged. Using LCD spot, lines and contamination standards. 8.3 Backlight doesn't light or color wrong.	0.65 2.5 0.65
09	Bezel	9.1 Bezel may not have rust, be deformed or have fingerprints, stains or other contamination. 9.2 Bezel must comply with job specifications.	2.5 0.65
10	PCB、COB	10.1 COB seal may not have pinholes larger than 0.2mm or contamination. 10.2 COB seal surface may not have pinholes through to the IC. 10.3 The height of the COB should not exceed the height indicated in the assembly diagram. 10.4 There may not be more than 2mm of sealant outside the seal area on the PCB. And there should be no more than three places. 10.5 No oxidation or contamination PCB terminals. 10.6 Parts on PCB must be the same as on the production characteristic chart. There should be no wrong parts, missing parts or excess parts. 10.7 The jumper on the PCB should conform to the product characteristic chart. 10.8 If solder gets on bezel tab pads, LED pad, zebra pad or screw hold pad, make sure it is smoothed down. 10.9 The Scraping testing standard for Copper Coating of PCB  $X * Y \leq 2mm^2$	2.5 2.5 0.65 2.5 2.5 0.65 0.65 2.5 2.5
11	Soldering	11.1 No un-melted solder paste may be present on the PCB. 11.2 No cold solder joints, missing solder connections, oxidation or icicle. 11.3 No residue or solder balls on PCB. 11.4 No short circuits in components on PCB.	2.5 2.5 2.5 0.65



NO	Item	Criterion	AQL
12	General appearance	12.1 No oxidation, contamination, curves or, bends on interface Pin (OLB) of TCP.	2.5
		12.2 No cracks on interface pin (OLB) of TCP.	0.65
		12.3 No contamination, solder residue or solder balls on product.	2.5
		12.4 The IC on the TCP may not be damaged, circuits.	2.5
		12.5 The uppermost edge of the protective strip on the interface pin must be present or look as if it cause the interface pin to sever.	2.5
		12.6 The residual rosin or tin oil of soldering (component or chip component) is not burned into brown or black color.	2.5
		12.7 Sealant on top of the ITO circuit has not hardened.	0.65
		12.8 Pin type must match type in specification sheet.	0.65
		12.9 LCD pin loose or missing pins.	0.65
		12.10 Product packaging must the same as specified on packaging specification sheet.	0.65
		12.11 Product dimension and structure must conform to product specification sheet.	



1. Material List of Components for RoHs

1. WINSTAR Display Co., Ltd hereby declares that all of or part of products (with the mark “#”in code), including, but not limited to, the LCM, accessories or packages, manufactured and/or delivered to your company (including your subsidiaries and affiliated company) directly or indirectly by our company (including our subsidiaries or affiliated companies) do not intentionally contain any of the substances listed in all applicable EU directives and regulations, including the following substances.

Exhibit A : The Harmful Material List

Material	(Cd)	(Pb)	(Hg)	(Cr6+)	PBBs	PBDEs
Limited Value	100 ppm	1000 ppm	1000 ppm	1000 ppm	1000 ppm	1000 ppm
Above limited value is set up according to RoHS.						

2.Process for RoHS requirement :

(1) Use the Sn/Ag/Cu soldering surface ; the surface of Pb-free solder is rougher than we used before.

(2) Heat-resistance temp. :

Reflow : 250°C,30 seconds Max. ;

Connector soldering wave or hand soldering : 320°C, 10 seconds max.

(3) Temp. curve of reflow, max. Temp. : 235±5°C ;

Recommended customer’s soldering temp. of connector : 280°C, 3 seconds.